MIM WEBINARS

AN IN-MEMORY COMPUTING SERIES

Next Talk: 04/April/2022, 4-5:30pm CET

TEST AND RELIABILITY ASPECTS OF COMPUTATION IN MEMORY

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Computation-in-Memory (CiM) paradigms are providing promising alternatives to tackle memory wall and power wall. CiM architectures based on emerging resistive non-volatile technologies are finding their way to efficiently implement deep learning cognitive tasks. Such technologies combine the storage and computation capabilities into the single device based on analog computing concepts. While many emerging technologies are being investigated for efficient implementation of such architectures and paradigms, there are several challenges related to test and reliability aspects of these technologies and architectures. From one side, these emerging devices are more prone to variations and defects, and from the other side, CiM paradigms crosses computation and storage boundaries, which were considered separated in traditional design-for-test (DfT) and design-for-reliability (DfR) solutions. This talk addresses design, test and reliability aspects of CiM technologies, circuits and architectures.

More information about the event and the speaker: https://www.ict.tuwien.ac.at/staff/taherinejad/MiM/next.html

Mondays in Memory (MIM) is a free biweekly webinar series open to everyone around the world and dedicated to all aspects and technologies related to in-memory computing (including, in a broader sense, near-memory computing too). MIM will be held on the first and third Monday of each month (since May 2021) at 4pm CET (7am Pacific time, and 10pm Beijing time).
Each webinar starts with a 40mins talk by a speaker, followed up with a 40mins questions and discussions with the speaker and two panel members. Dr. Nima Taherinejad hosts the webinars, and together with his team they organize the MiM series.

Website: http://www.ict.tuwien.ac.at/staff/ aherinejad/MiM/
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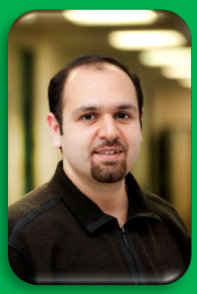

Mehdi Tahoori is Professor and the Chair of Dependable Nano-Computing at Karlsruhe Institute of Technology, Germany. He received the B.S. degree in computer engineering from Sharif University of Technology, Tehran, Iran, in 2000, and the M.S. and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, in 2002 and 2003, respectively. In 2003, he was an Assistant Professor at Northeastern University, where he became an Associate Professor in 2009. He was a visiting professor at University of Tokyo, Japan in 2015. From 2002 to 2003, he was a Research Scientist with Fujitsu Laboratories of America, Sunnyvale, CA. He has authored over 400 publications in major journals and conference proceedings on a wide range of topics, from dependable computing and emerging nanotechnologies to system biology, and holds several US and European patents. He is currently the deputy editor-in-chief of IEEE Design and Test Magazine. He is a fellow of IEEE.